AF/2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Group Art Unit: 2814
Examiner: Mr. Nathan W. Ha

In re PATENT APPLICATION of:

Applicant(s)	:	Makoto TERUI et al.
Serial No.	:	10/022,268
Filed	:	December 20, 2001
For	:	SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATING SAME
Attorney Ref.	:	OKI 286

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certification Under 37 C.F.R. §1.8 (if applicable)

I hereby certify that this Appeal Brief (in triplicate) is being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. §1.8 on this **October 14, 2003** and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Pamela J. Ledford
Typed or printed name of person mailing the Amendment and Petition for Extension of Time

Signature of person mailing the Amendment and Petition for Extension of Time

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Group Art Unit: 2814
Examiner: Mr. Nathan W. Ha

In re PATENT APPLICATION of:

Applicant(s)	:	Makoto TERUI et al.
Serial No.	:	10/022,268
Filed	:	December 20, 2001
For	:	SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATING SAME
Attorney Ref.	:	OKI 286

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal to the Board of Patent Appeals and Interferences from the decision, in the Office Action of April 14, 2003, finally rejecting claims 9-21. A Notice of Appeal (plus a Petition for a one month extension of time) were filed on August 14, 2003. Accordingly, it is respectfully submitted that this Brief is timely. This Brief is being submitted in triplicate.

(1) REAL PARTY IN INTEREST

The real party in interest in this appeal is Oki Electric Industry Co., Ltd., having an office at 7-12, Toranomon 1-chome, Minato-ku, Tokyo, Japan.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

(3) STATUS OF CLAIMS

The claims involved in this appeal are set forth in an Appendix to this Brief. Claims 9-21 have been finally rejected and are being appealed. Claims 1-8 were withdrawn from consideration as a result of a restriction requirement and were subsequently cancelled. No claims have been allowed.

(4) STATUS OF AMENDMENTS

A paper entitled "Request for Supplemental Office Action" was filed on April 25, 2003 in order to seek clarification of a rejection for new matter in the Office Action of April 14, 2003. An Advisory Action dated May 19, 2003 withdrew the new matter rejection.

A paper entitled "Response After Final Rejection" was filed on June 23, 2003 to traverse a rejection for obviousness. However, an Advisory Action dated July 28, 2003 reported that claims 9-21 remained finally rejected.

(5) SUMMARY OF THE INVENTION

The present application discloses several embodiments of a method for fabricating a semiconductor package. In the embodiment shown in Figures 1(A)-1(C), a solder ball 14 is placed in a recess 15 in a lower molding die member 10b. Reference number 28b represents a plastic layer on the die member 10b. A lead frame 17 having a

protrusion 25 is disposed over the die member 10b, while an upper molding die member 10a is disposed over the lead frame 17. The member 10a, which likewise has a plastic layer on it, includes a press-down part 16.

The die members 10a and 10b are pre-heated, for example to a temperature in the range of 150°C-220°C, and the mold is closed (see page 10 of the application, lines 3-12). As is shown in Figure 1(B), the press-down part 16 forces the protrusion 25 on the lead frame to penetrate the solder ball 14. Resin material is then injected to form a sealing member 29, as shown in Figure 1(C).

Since the solder balls 14 are exposed to the atmosphere at a high temperature only during the clamping step, the growth of oxide films on the solder balls is reduced in comparison with conventional manufacturing methods (page 12, lines 14-17).

In the embodiment shown in Figures 3(A)-3(C), the lead frame 17 is provided with a solder layer 125. In the embodiment shown in Figure 5, the lead frame has a roughened region 225 to promote bonding. In the embodiment shown in Figure 6(A)-6(C), negative pressure is applied to the solder ball via a path 32. Negative pressure is also applied in the embodiment shown in Figures 7(A)-7(C).

(6) ISSUE

The following issue is presented to the Board: whether claims 9-21 have been properly rejected for obviousness on the basis of U.S. patent 6,187,612 to Orcutt in view of published U.S. application 2002/0027441 to Akram et al (hereafter simply "Akram").

(7) GROUPING OF CLAIMS

The claims do not stand or fall together. Instead, independent claims 9, 12, 14, 15, and 18 are believed to be separately patentable for the reasons presented in this brief. Furthermore, dependent claims 13, 16, 17, and 19-21 are believed to be separately patentable. The rejection of the remaining dependent claims will not be separately contested herein, and thus, for purposes of the present appeal only and without waiving any future rights, the remaining dependent claims may be deemed to stand or fall together with their independent claims.

(8) ARGUMENT

Since the claims on appeal have all been rejected for obviousness on the basis of Orcutt in view of Akram, it is appropriate to begin with a brief summary of what these references disclose.

The Disclosures of the References

In Figure 3 of Orcutt (the same figure that is reproduced on the cover sheet of the reference), a depending finger 9 on an upper mold die 7 causes a material 3 beneath a solder ball 5 to be deformed (see the Abstract of the reference). Reference number 11 identifies a lead frame.

The Akram reference is directed to an "interconnect" (see reference number 10 in Akram's Figure 1) that is used during testing of semiconductor components. Figure 5 of the reference shows a cross section of a portion of the substrate 12 of the interconnect. It

includes a flexible segment 26C beneath a recess 38B. A projection 48 is formed in the recess. A conductive layer 30B that is provided on the "interconnect" engages a bumped contact 16 on a component 18 that is to be tested. (See paragraphs [0043], [0044], [0071], and [0072].)

The arrangement shown in Akram's Figure 7F includes a pressure conduit 40 (see paragraph [0084]).

Akram is in a Non-analogous Art

It is respectfully submitted that the Akram reference is in an non-analogous art, so that a person who is ordinarily skilled in the semiconductor packaging art should not be presumed to know that Akram even exists. At the bottom of page 4, the Office Action of April 14, 2003 (which will hereafter be called the Final Rejection) comments that Akram teaches a semiconductor package. The fact remains, though, that the reference itself advises that it "relates generally to semiconductor testing ..." (see paragraph [0002]). The mere fact that a packaged semiconductor appears in the Akram reference would not be enough to attract the attention of the person who is ordinarily skilled in the semiconductor packaging art. It is well known that packaged semiconductors are used in the radar art, the radio art, the computer art, and many other arts. An ordinarily skilled person who wanted to make an improvement in semiconductor packaging would have no more reason to refer to the semiconductor testing art than to all these other arts that use packaged semiconductor devices.

The Independent Claims

In **independent claim 9**, steps (a) and (e) refer to a lead frame that has a protrusion. Similarly, steps (b) and (c) of **independent claim 18** refer to a lead frame having a protrusion. The Final Rejection acknowledges that Orcutt does not disclose such a protrusion. However, at the middle of page 3 the Final Rejection takes the position that Akram:

> "discloses an analogous semiconductor packaging with a lead frame 12A with a protrusion 48 with an acute angle. This protrusion is provided to make a better electrical contact between the substrate and the solder ball since it increases the contact surface area."

Later, in the "Response to Arguments" section, the Final Rejection takes the position that Akram's "substrate 12 can be used as a frame since it carries electrical conductors on the surface, for example, element 32B...".

Applicants respectfully disagree. The term "lead frame" is well known in the semiconductor packaging art. The term refers to a metal frame that is used to hold leads in place while a chip is encapsulated, and is then trimmed to disconnect the leads from one another. An ordinarily skilled person would not consider Akram's substrate 12 to be a lead frame. Instead, it is part of a connection arrangement (see Akram's Figure 1) for testing semiconductors after the leads have been attached and wired to the chip. It should be noted that the solder ball 16 shown in Akram's Figure 5 is already connected to the pad 19 of Akram's component 18 *before* the component 18 is tested using Akram's interconnection arrangement.

As was noted above, the Final Rejection takes the position that Akram's protrusion is provided to make better electrical contact between the substrate and the solder ball since it increases the contact surface area. However, there is no evidence of record that poor electrical contact between solder balls and the leads of a lead frame has ever been recognized as a problem in the semiconductor packaging art. Consequently, there is no reason why an ordinarily skilled person would have been motivated to increase the contact surface area between solder balls and leads of a lead frame.

Independent claim 12 refers to a locally roughened face in steps (a), (e), and in a final "wherein" clause. Neither reference discloses or suggests a lead frame with a locally roughened face that is pressed against a terminal.

Independent claim 14 recites the step of "absorbing air existing between said substantially spherical terminal and said bottom of said cavity" via a hole in a first mold "to urge said substantially spherical terminal against the inner side of said cavity." Similarly, **independent claim 15** recites "exposing a bottom portion of said substantially spherical terminal to reduced pressure via said through hole in the bottom of the cavity so as to urge said substantially spherical terminal against an inner wall of said cavity." At the bottom of page 3, the Final Rejection comments that Akram's Figure 7F shows a throughhole 40 in the substrate. The Final Rejection then states, "this throughhole is used to inject or suck out air, gas, or liquid pressure in the cavity," and takes the position that it would have been obvious to use Akram's throughhole in Orcutt's arrangement in order to take full advantage. The trouble with this position is that Akram only teaches injecting a substance **into** a cavity using a throughhole (see paragraph [0084] of the Akram reference, for example) and the purpose of this is to exert an upward force on the bottom

side of the cavity (see paragraphs [0066] and [0067] of the reference). There is no hint in the reference of using Akram's throughhole 40 to suck air, gas, or liquid **out** of the cavity.

The Dependent Claims

Since the remaining claims that have been rejected depend from the independent claims discussed above and recite additional limitations to further define the invention, they are patentable along with their independent claims. Several of the dependent claims, however, will now be individually addressed.

Claim 13, which depends from claim 9, recites the step of "sucking in the substantially spherical terminal via a through hole in the bottom of the cavity of the first molding die member." As was noted above, pressure is exerted through the conduit 40 in Arkam's Figure 7F, not suction.

Claim 16, which depends from claim 11, recites that a step of causing the protrusion to pierce the substantially spherical terminal "comprises pressing against the lead frame with a press-down part ...". In contrast, Orcutt uses his depending finger 9 to press against his lead frame 11 only for the purpose of deforming his material 3 beneath his solder ball 5.

Claim 17, which depends from claim 9, recites "causing the solder layer to press against the substantially spherical terminal." Neither reference suggests pressing a solder layer on a lead frame against a substantially spherical terminal.

Claim 19, which depends from claim 18, provides that a protrusion "is driven into the solder ball" while mold dies are moved to their closed state. This is not suggested by the references.

Claim 20, which also depends from claim 18, provides that a solder layer is pressed against a solder ball while mold dies are moved to their closed state. It is respectfully submitted that the references contain no hint of this.

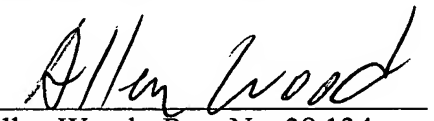
Finally, **claim 21**, which depends from claim 18, provides that a solder ball is exposed to reduced pressure via a passage. At the risk of being redundant, it is noted again that Akram applies increased pressure in his Figure 7F, not reduced pressure.

Conclusion

For the foregoing reasons, it is respectfully submitted that the rejected claims are patentable over Orcutt and Arkam. Accordingly, the Examiner's rejection of the claims should be reversed.

The applicable Appeal Brief fee of $330 is being submitted concurrently. Should this remittance be accidentally missing, however, or should any additional fees be needed, such fees may be charged to our Deposit Account number 18-0002.

Respectfully submitted,



October 14, 2003
Date

Allen Wood - Reg. No. 28,134
RABIN & BERDO, P.C.
Telephone: 202-371-8976
Telefax: 202-408-0924
CUSTOMER NO. 23995

AW/rw

(9) APPENDIX

Claims on Appeal

Claims 1-8 have been cancelled.

9. A method of fabricating a semiconductor package, comprising:

(a) preparing a lead frame that has a protrusion;

(b) preparing a first molding member having a cavity;

(c) preparing a second molding member to be engaged with the first molding member;

(d) disposing a substantially spherical terminal in the cavity;

(e) holding the lead frame between the first and second molding members such that the protrusion is disposed opposite to the substantially spherical terminal; and

(f) a step of injecting a molding composition between the first and second molding members.

10. A method of fabricating a semiconductor package according to claim 9, wherein the substantially spherical terminal comes to be in intimate contact with the sidewall of the cavity in step (e).

11. A method of fabricating a semiconductor package according to claim 9, wherein the protrusion has an extremity forming an acute angle, and wherein step (e) further comprises causing the protrusion to pierce the substantially spherical terminal.

12. A method of fabricating a semiconductor package comprising:

(a) preparing a lead frame that has a locally roughened face;

(b) preparing a first molding member having a cavity;

(c) preparing a second molding member to be engaged with the first molding member;

(d) disposing a substantially spherical terminal in the cavity;

(e) holding the lead frame between the first and second molding members such that the locally roughened face is disposed opposite to the substantially spherical terminal; and

(f) injecting a molding composition between the first and second molding members,

wherein step (e) further comprises causing the locally roughened face to press against the substantially spherical terminal.

13. A method of fabricating a semiconductor package according to claim 9, further comprising the step of sucking in the substantially spherical terminal via a through hole in the bottom of the cavity of the first molding member.

14. A method of forming a semiconductor package which comprises the steps of:

preparing a lead frame having a substantially spherical terminal;

preparing a first mold having a cavity with a through hole in the bottom thereof;

preparing a second mold for matching with said first molding ;

placing said lead frame between said first and second mold s, wherein said substantially spherical terminal of said lead frame is placed in said cavity;

absorbing air existing between said substantially spherical terminal and said bottom of said cavity via said through hole to urge said substantially spherical terminal against the inner side of said cavity; and

injecting a molding composition between said first and second mold s.

15. A method of forming a semiconductor package which comprises the steps of:

preparing a lead frame having a substantially spherical terminal;

preparing a first mold having a cavity with a through hole in the bottom thereof;

preparing a second mold for matching with said first molding ;

placing said lead frame between said first and second mold s, wherein said substantially spherical terminal of said lead frame is placed in said cavity;

bringing said first and second mold;

exposing a bottom portion of said substantially spherical terminal to reduced pressure via said through hole in the bottom of the cavity so as to urge said substantially spherical terminal against an inner side of said cavity; and

injecting a molding composition between said first and second mold s.

16. The method of fabricating a semiconductor package according to claim 11, wherein the step of causing the protrusion to pierce the substantially spherical terminal comprises pressing against the lead frame with a press-down part of the second molding .

17. The method of fabricating a semiconductor package according to claim 9, wherein the lead frame has a bottom side and the protrusion comprises a solder layer on a portion of the bottom side of the lead frame, and wherein step (e) further comprises causing the solder layer to press against the substantially spherical terminal.

18. A method of fabricating a semiconductor package using a mold having upper and lower mold s that are movable between an open state and a closed state, the mold s defining a mold cavity when they are in their closed state, said method comprising:

(a) while the mold s are in their open state, placing a solder ball in a recess of a lower molding ;

(b) while the mold s are in their open state, placing a lead frame above the lower molding , with the lead frame having a lead that passes over the solder ball, the lead having a bottom side with a downwardly extending protrusion;

(c) moving the mold s to their closed state, and simultaneously pressing the protrusion against the solder ball by pressing a hold-down part of the upper mold against the lead, the hold-down part being located over the solder ball; and

(d) injecting a molding composition into the mold cavity.

19. A method of fabricating a semiconductor package according to claim 18, wherein the protrusion is elongated in a downward direction, and is driven into the solder ball as step (c) is being conducted.

20. A method of fabricating a semiconductor package according to claim 18, wherein the protrusion is a small solder layer that is pressed against the solder ball during step (c).

21. A method of fabricating a semiconductor package according to claim 18, wherein the lower mold has a passage that communicates with the recess, and further comprising the step of exposing the solder ball to reduced pressure via the passage so as to urge the solder ball tightly into the recess.